US005781768A

United States Patent [19]

Jones, Jr.

[11] Patent Number: 5,781,768

[45] Date of Patent: Jul. 14, 1998

[54] **GRAPHICS CONTROLLER UTILIZING A VARIABLE FREQUENCY CLOCK**

[75] Inventor: **Morris E. Jones, Jr.**, Saratoga, Calif.

[73] Assignee: **Chips and Technologies, Inc.**, San Jose, Calif.

[21] Appl. No.: **625,732**

[22] Filed: **Mar. 29, 1996**

[51] **Int. Cl.**[6] **G06F 1/06**

[52] **U.S. Cl.** **395/556**

[58] **Field of Search** 395/556

[56] **References Cited**

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5,285,197	2/1994	Schmidt et al.	345/213
5,481,697	1/1996	Mathews et al.	395/556
5,586,309	12/1996	Lin	395/556

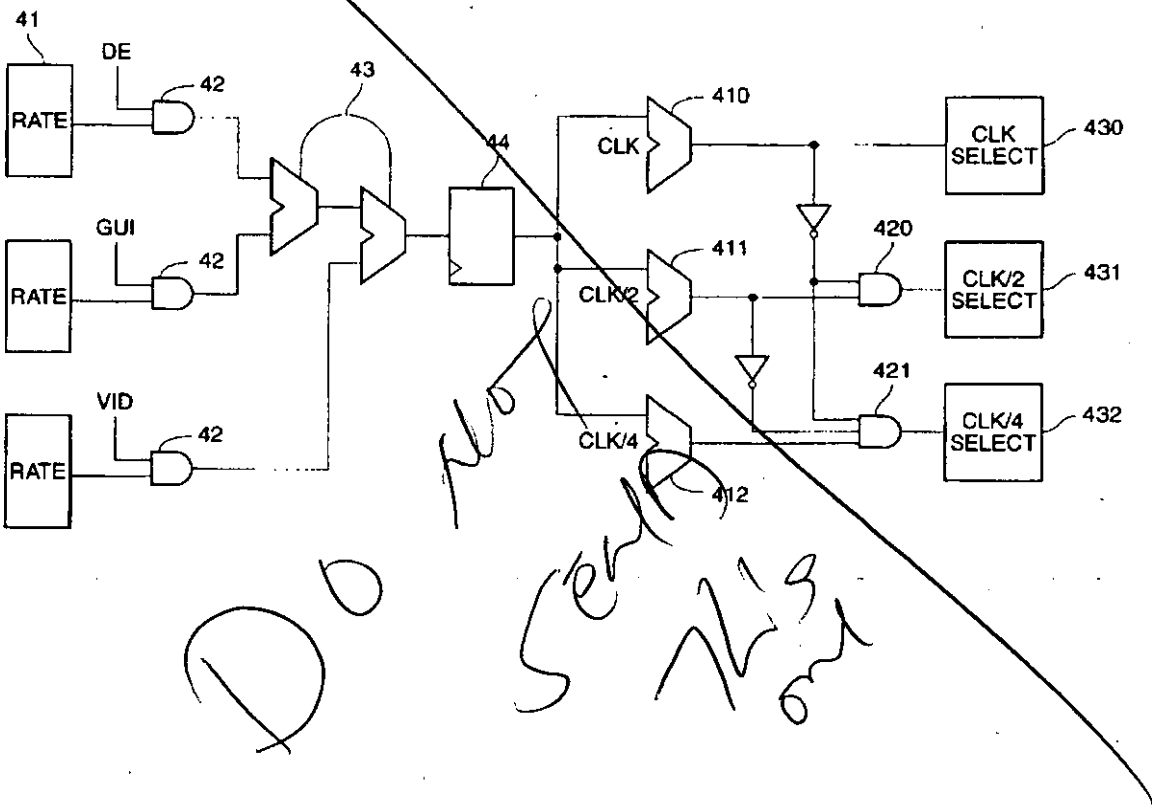
Primary Examiner—Thomas M. Heckler

Attorney, Agent, or Firm—D'Alessandro & Ritchie

[57] **ABSTRACT**

The present invention includes a memory clock system for a graphics controller including a plurality of clock pulse generators, and a clock controller which selects the clock frequency based on the state of the graphics controller functional units.

5 Claims, 2 Drawing Sheets



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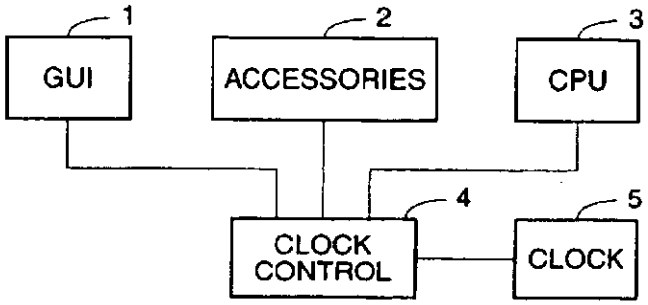


FIG. 1

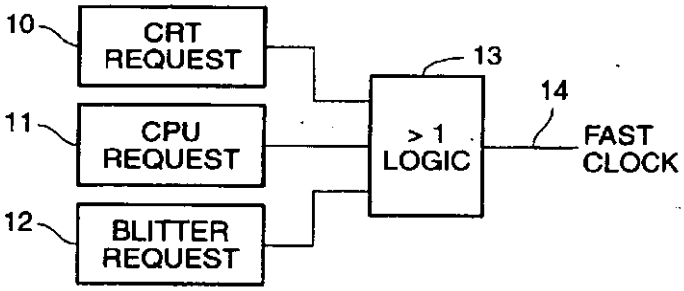


FIG. 2

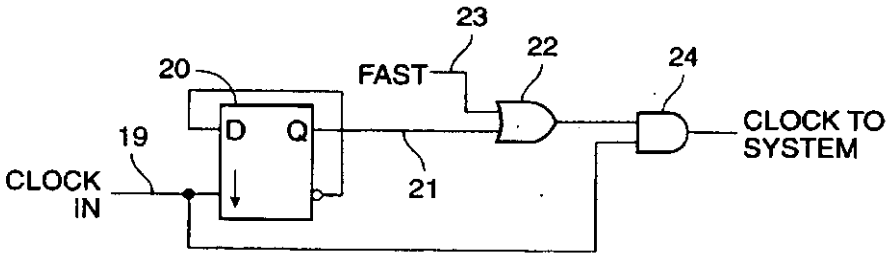


FIG. 3

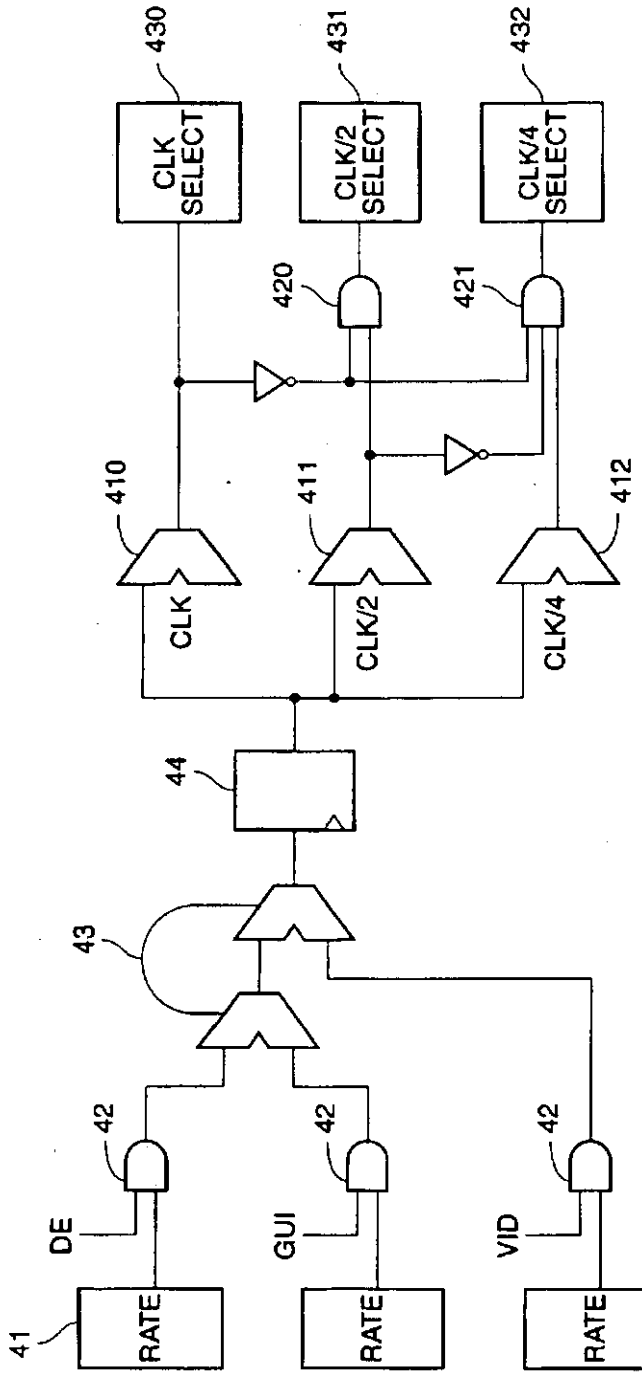

430
431
432
CLK SELECT
CLK/2 SELECT
CLK/4 SELECT
420
421
410
411
412
CLK
CLK/2
CLK/4
44
43
42
42
42
DE
GUI
VID
41
RATE
RATE
RATE

FIG. 4

required for $B_{display}$ is required in addition the frequency required for $B_{display}$. Thus, the average frequency requirement is 0.5 +0.175 =0.675, or 68% of the typical engineered frequency. Operating the clock at this average frequency would result in a reduction of 32% in bandwidth, and in a proportional reduction in power consumption in the graphics controller.

FIG. 1 shows a general system for implementing frequency reduction based on the activity level of the system.

Each major functional unit, including GUI 1, Accessories 2 and CPU 3, provides a signal to a Clock Control 4 indicating whether the respective functional unit is active or inactive, and Clock Control 4 selects an appropriate signal to Clock 5 based on the programming of Clock Control 4 and the amount and type of activity. In a simple system, Clock Control 4 would be programmed so that, when there is no activity, the frequency would be the maximum engineered rate divided by two (enough for the display only), and when any activity occurs, the frequency would be the maximum engineered clock rate. Systems utilizing more complex clock control schemes could also be used. More than two clock control speeds could be selected based on the number of functional units active at a given time or based on which specific functional units are active. Continuous clock variation could also be used if warranted by the application.

The activity of each functional unit may be indicated by the functional units not being idle, by FIFO depths in each functional unit, and by the position of the display beam for multi-media and popup accessories.

Other data may be sent to Clock Control as a basis for clock frequency adjustment. In the analysis above, $B_{display}$ was considered to be constantly utilized at a 100% rate, but the display is not uniform in memory bandwidth requirements, and an improvement can be made that allows the M clock to be reduced during the blanking intervals when the display is not fetching any data. This could reduce the power consumption another 5–10% depending on the graphics timing of the display.

FIG. 2 shows a preferred embodiment of a clock controller. A typical graphics controller contains several functional units communicating with the memory controller. These typically have a request mechanism. The memory clock may be changed based on the number of pending requests. The CRT Request 10 represents a memory access request from the CRT display engine, the CPU Request 11 represents a request from the CPU or Bus interface, and the Blitter Request 12 represents a request from graphics acceleration logic such as BitBlt or line draw hardware.

The >1 logic block 13 can be implemented by the following truth table:

CRT	CPU	Blt	Fast
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Since the clock required when the CPU and/or Blitter are operating is normally twice the CRT only clock, the circuit shown in FIG. 3 could be used to implement the clock switching. Clock In 19 is the system clock engineered for the worst case scenario. Flip flop 20 outputs at line 21 a signal at half the clock frequency. OR gate 22 outputs either a constant high signal or the half frequency signal depending on whether the Fast Input 23 is enabled. AND gate 24 outputs a signal that is either half the frequency of Clock In 19 or the same frequency as Clock In 19 depending on the state of the Fast Input 23. Thus, when the fast mode is enabled, every clock pulse will be let through, when it is not, then every second clock pulse will be let through. This circuit should reduce the power consumption in the chip considerably.

A more complex clock control scheme may be designed using the bandwidth requirements of each function. For example, the following bandwidths may be required:

Horizontal and vertical Display Enable (DE) - 85 Mb/sec when active

GUI Engine (GUI)- 100 Mb/sec when active

Video (VID) - 28 Mb/sec when active.

The appropriate clock frequency may be selected from among, for example, CLK =220 Mb/sec, CLK/2=110 Mb/sec and CLK/4=55 Mb/sec, based on the total bandwidth required as follows:

DE	GUI	VID	BW	CLK = 220 Mb/sec	CLK/2 = 110 Mb/sec	CLK/4 = 55 Mb/sec
0	0	0	0			✓
0	0	1	28			✓
0	1	0	100	✓		
0	1	1	128	✓		
1	0	0	85		✓	
1	0	1	113	✓		
1	1	0	185	✓		
1	1	1	213	✓		

The clock select signals may then be generated by:

$CLK = DE \cdot GUI + \overline{VID} \cdot GUI + DE \cdot VID$

$CLK/2 = \overline{DE} \cdot GUI \cdot \overline{VID} + DE \cdot \overline{GUI} \cdot VID$

$CLK/4 = \overline{DE} \cdot GUI$

It will be apparent to one of ordinary skill in the art that the following design could be modified to adjust to other requirements. Alternatively, adders could be used as shown in FIG. 4.

Programmable rate inputs 41 are input to AND gates 42, along with enable signals from DE, GUI, and VID. The outputs from the AND gates are routed through adders 43 and through cycle point 44, if needed, to comparators 410, 411 and 412. The other inputs to comparators 410, 411 and 412 are the minimum rates for which the CLK, CLK/2, and CLK/4 signals are respectively required.

AND gates 420 and 421 determine the proper clock select signals to clocks CLK, CLK/2 and CLK/4. Cycle points 430, 431 and 432 are used if necessary. Alternatively, the control signals could be input to a Phase Locked Loop. In the example shown, the clock rates used were CLK, CLK/2 and CLK/4. Alternatively, fully programmable clock rates could be used.

In general, each functional unit has a state machine. These state machines can indicate when the unit is busy. This allows a speed up when internal processing is occurring, and not just when the memory controller is busy. Graphics chips are typically composed of a number of functions. These include Hardware cursors and popup menus that fetch data from system memory. These are active for a very short period each screen refresh. These units can also indicate when they are active, and increase the memory clock.

If a large number of functional units are present in the chip, then a system with multiple clock speeds can be implemented. The other units typically do not add up to a multiple of the CRT bandwidth requirement. This would

require a second clock frequency source, or fast changing phase locked loop for efficient implementation. Some examples of other functions' bandwidth are:

Function	Bandwidth Mb/Sec
Multi-media in	4.61
Multi-media out	11.52
Cursor sprite	0.02
Pop-up Menu	0.31
Total	16.45

If a design included multi-media in, then a system could be constructed so that a slow clock is used whenever the Multimedia input and CRT are the only components operating. Such a system would switch to the fast mode only if the sum of the bandwidths exceeded the memory system capacity in the slow clock. The conditions for a fast or slow clock would be captured in logic, stored in a RAM, or implemented in a ROM, and then used to select the system operating speed. The conditions and logic implementation ensure that the bandwidths required meet the system requirements.

In summary, an apparatus and method for providing a variable memory clock in a graphics controller has been described.

The foregoing description of the preferred embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and many modifications and variations are possible in light of the above teaching. The preferred embodiment was chosen and described in order to best explain the principles of the invention and its practical applications to thereby enable others skilled in the art to best utilize the invention and various embodiments, and with various modifications as are suited to the particular use contemplated.

It is intended that the scope of the invention be defined only by the appended claims.

What is claimed is:

1. A memory clock system for a graphics controller having functional units which includes: a plurality of clock pulse generators, a clock controller including,

input lines having a state, said state being determined by the activity of said functional units,

clock control logic circuitry responsive to the state of said input lines,

an output signal line, said output signal line connected to each of said plurality of clock pulse generators wherein the clock control logic circuitry sends a signal on the output signal line, the signal indicating which of the clock pulse generators is to be active, whereby said clock controller causes said plurality of clock pulse generators to generate clock pulses at a predetermined frequency for use by the graphics controller based on the state of said functional units.

2. The clock system of claim 1 wherein the state of the input lines is further determined by the bandwidth requirements of the functional units.

3. A memory clock system for a graphics controller as recited in claim 1 wherein the functional units include a graphics accelerator engine, a CPU, and accessory function.

4. A memory clock system for a graphics controller as recited in claim 1 wherein the plurality of clock pulse generators includes a slow clock pulse generator and a fast clock pulse generator and wherein the clock control logic circuitry causes the slow clock pulse generator to generate clock pulses when at least one of the functional units is active and wherein the clock control logic circuitry causes the fast clock pulse generator to generate clock pulses when none of the functional units are active.

5. A memory clock system for a graphics controller having functional units which includes: a variable clock pulse generator, a clock controller including,

input lines having a state, said state being determined by the activity of said functional units,

clock control logic circuitry responsive to the state of said input lines,

an output signal line, said output signal line connected to the variable clock pulse generator, wherein the clock control logic circuitry sends a signal on the output signal line the signal indicating a clock frequency to be generated by the variable clock pulse generator, whereby said clock controller causes said variable clock pulse generator to generate variable rate clock pulses for use by the graphics controller based on the state of said functional units.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,781,768
DATED : July 14, 1998
INVENTOR(S) : Morris E. Jones

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

---At column 1, line 24, replace i~CVF," with --i ~ CVF--.

---At column 1, line 26, replace "p~CV^{2}F," with --p ~ CV^{2}F--.

---At column 1, line 50, replace "K_{bW}" with --K_{bw}--.

---At column 1, line 50, replace "B_{cpu}" with --B_{CPU}--.

---At column 1, line 50, replace "B_{GUi} with --B_{GUI}--.

---At column 2, line 64, replace "B_{cpu}" with --B_{CPU}--.

---At column 2, line 64, replace "B_{GUi}" with -- B_{GUI}--.

---At column 4, line 27, delete "√" from the row starting with "0 1 0 100" and the column starting with "CLK =".

---At column 4, ine 27, insert "√" in the row starting with "0 1 0 100" and the column starting with "CLK/2 =".

---At column 6, line 40, after "line" insert --,--.

Signed and Sealed this

Twelfth Day of January, 1999

Attest:

Attesting Officer

Acting Commissioner of Patents and Trademarks

GRAPHICS CONTROLLER UTILIZING A VARIABLE FREQUENCY CLOCK

BACKGROUND OF THE INVENTION

The present invention relates generally to a system and method for providing multiple clock rates for a graphics controller depending on what functions are being performed at a given time.

Prior art graphics controllers use memory clocks which operate at only a single frequency. A preferred embodiment of the present invention recognizes the direct relationship between memory clock frequency and power consumption and uses a variable frequency memory clock to reduce power consumption.

The power consumed by a chip is the current consumed by the chip multiplied by the voltage at which the chip operates, or:

$$P=IV,$$

The current consumed by a chip is directly related to capacitance, voltage, and frequency as follows:

$$i=CVF,$$

The power consumed by the chip is therefore:

$$p=CV^2F,$$

Thus, power consumption may be reduced by either reducing the capacitance of the devices on the chip, the voltage on the chip, or the frequency at which the chip operates. The capacitance is related to the devices which are constructed on the chip. The number and type of devices required on the chip are determined by the functions which the chip must perform. In most cases, it is fixed by the required product function. The voltage on the chip may be varied, but product requirements usually fix it at approximately 3.3 Volts to facilitate interface to other components. The frequency is determined by the required memory bandwidth.

The goal in a flat panel graphics controller chip is to reduce the power consumption as much as possible. The capacitance and voltage of the chip are generally fixed by product requirements. Significant reduction in power consumption, however, could be accomplished if a way to reduce the required memory bandwidth and therefore the frequency were provided.

The required frequency of operation of a graphics chip is given by the following expression:

$$F=K_{bw}*(B_{display}+B_{cpu}+B_{GUI}+B_{acc}),$$

Where:

K_{bw}	Constant to convert bandwidth to frequency. Determined by the architecture of the memory controller.
$B_{display}$	Bandwidth required to display the screen data
B_{CPU}	Bandwidth required for CPU functions (Performance related)
B_{GUI}	Bandwidth required for screen manipulation by the graphics acceleration engine in addition to the CPU bandwidth. (Performance related)
B_{acc}	Bandwidth required for accessory functions such as cursors, pop up windows, multi-media, DRAM refresh, and storage buffers for dual drive flat panels displays.

Prior art systems are engineered to provide enough bandwidth to handle the maximum possible total bandwidth

requirement. This is typically about twice the display bandwidth. Prior art systems are engineered for this worst case environment, and the clock rate is set accordingly. During periods when the bandwidth requirement of the system is reduced, the clock rate still remains set at the rate determined by the maximum bandwidth requirement. Power consumption could be reduced if a lower clock rate than the clock rate engineered for the maximum bandwidth requirement could be used when the bandwidth requirement is less than the maximum.

SUMMARY OF THE INVENTION

Accordingly, the present invention provides a system and method of using multiple clock rates that are selected based on the functions being performed by the graphics chip at a given time. The clock rate selected provides adequate bandwidth for the functions provided without any loss in performance. Intermittent use of a lower clock rate results in lower overall power consumption by the graphics controller.

Additional objects and advantages of the invention will be set forth in part in the description which follows, and will become apparent to those skilled in the art upon examination of the following, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, schematically illustrate a preferred embodiment of the invention and, together with the general description given above and the detailed description of the preferred embodiment given below, serve to explain the principles of the invention.

FIG. 1 is a block diagram depicting a system for controlling the clock frequency.

FIG. 2 is a block diagram depicting a preferred embodiment of the clock control logic.

FIG. 3 is a block diagram depicting a preferred embodiment of the circuit used to switch the clock frequency.

FIG. 4 is a block diagram depicting a preferred embodiment of clock control logic.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the preferred embodiment of the invention, which is a system and method for providing a variable frequency clock for a graphics controller. An example of the preferred embodiment is illustrated in the accompanying drawings. While the invention will be described in conjunction with that preferred embodiment, it will be understood that it is not intended to limit the invention to one preferred embodiment. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

In a typical computer environment the screen is displayed at a 100% rate, the accessories are used about 15% of the time, and the CPU and GUI functions are used about 10% of the time. This results in an average frequency of:

$$F=K_{bw}*(B_{display}+.1*B_{cpu}+0.1*B_{GUI}+0.15*B_{acc})$$

Since the other factors are each about the same as $B_{display}$, approximately 0.35 * 0.5 or 0.175 times the frequency

US-PAT-NO: 6307281
DOCUMENT-IDENTIFIER: US 6307281 B1

TITLE: System and method for reducing power dissipation in a circuit

DATE-ISSUED: October 23, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Houston; Theodore W.	Richardson	TX	N/A	N/A

US-CL-CURRENT: 307/31,307/39

ABSTRACT:
A method for selective allocation of power to elements of a circuit comprises identifying at least one element of the circuit for reduced power dissipation and selecting the at least one element. The method further comprises altering an input to the at least one element thereby reducing the power dissipated by the at least one element.

26 Claims, 9 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

FIG. 7

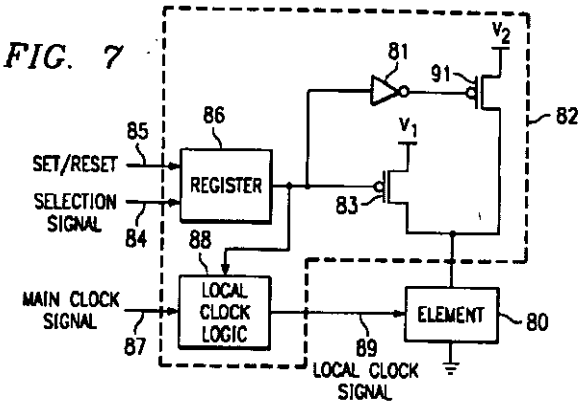


FIG. 8

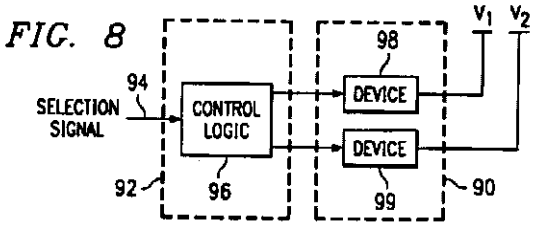
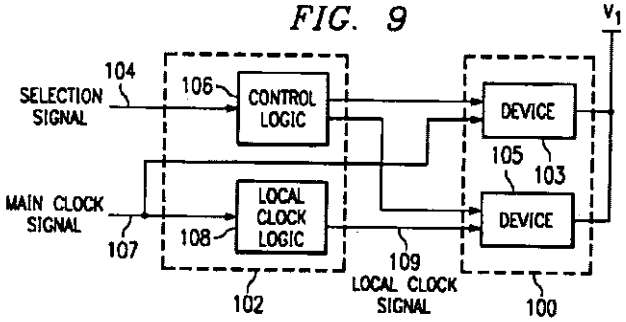


FIG. 9



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26 Claims, 9 Drawing figures
Exemplary Claim Number: 1
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ssipation is desired. It should be noted that the shift register can be utilized for operations other than multiplication, and is therefore not necessarily powered down when the multiplier is utilized. Additionally, in such an example a shift register/adder combination may be selected for multiplication when a multiplier has been previously powered down. To avoid having to delay operation while the multiplier is powered on, the shift register/adder is selected to perform an equivalent operation. Devices **98** and **99** may also each include a plurality of transistors, the transistors being used by one of devices **98** and **99** having a higher threshold voltage than the transistors being used by the other device. The device having transistors with a higher threshold voltage may be selected during intervals in which reduced power dissipation for element **90** is desired.

FIG. **9** is a block diagram of another embodiment of the present invention. An element **100** includes devices **103** and **105** as alternative and parallel data paths. Control interface **102** includes a control logic **106** that may include a register and a multiplexer. Control interface **102** further includes a local clock logic **108**. Control logic **106** receives selection signal **104** and generates two control output signals, one connected to each of devices **103** and **105**. Local clock logic **108** receives main clock signal **107** as an input and adjusts the frequency of main clock signal **107** to generate an output of a local clock signal **109** to device **105**. Device **103** uses main clock signal **107** as a clock input signal. Device **105** uses local clock signal **109** as a clock input signal. Both devices **103** and **105** are supplied by voltage signal V_1. Generally, control interface **102** selects device **103** or **105** within element **100** by altering the output control signals of control logic **106** in response to selection signal **104**. As devices **103** and **105** use different clock input signals operating on different clock frequencies, control interface **102** can adjust the amount of power dissipated by element **100**.

In operation, control logic **106** selects a particular device **103** or **105** to execute instructions or perform operations during a designated interval in response to selection signal **104**. Local clock logic **108** allows a lower frequency clock signal to be supplied to device **105** while device **103** retains the same frequency of clock input as main clock signal **107**. Element **100** may therefore operate in a reduced power dissipation mode by using the data path encompassed by device **105** rather than device **103**.

Devices **103** and **105** are supplied with an identical voltage input V_1. However, alternate voltage inputs could be provided for each device to offer an even greater differential in the power dissipated by devices **103** and **105**. Devices **103** and **105** can be identical or functionally equivalent devices or combinations of components as discussed above in reference to devices **98** and **99** of FIG. **8**. Thus, device **105** may have greatly reduced power dissipation by being composed of components dissipating less power than those in device **103**, being supplied with a lower frequency clock input and/or being supplied with a lower voltage input.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made therein without departing from the spirit and scope of the present invention as defined by the appended claims.

What is claimed is:

1. A method for selective allocation of power to elements of a circuit, comprising:

identifying at least one element of the circuit for reduced power dissipation;

selecting the identified at least one element; and

reducing the power supply voltage of the at least one element from a normal operating first voltage to a reduced power operating voltage less than the first voltage.

2. A method for selective allocation of power to elements of a circuit, comprising:

identifying at least one element of the circuit for reduced power dissipation;

selecting the identified at least one element; and

reducing the frequency of a clock signal input to the at least one element from a normal operating first frequency to a nonzero second frequency.

3. A method for selective allocation of power to elements of a circuit, comprising:

identifying at least one element of the circuit for reduced power dissipation comprising identifying at least one transistor;

selecting the identified at least one element; and

changing a threshold voltage of the identified transistor.

4. A method for selective allocation of power to elements of a circuit, comprising:

identifying a first device and a second device coupled in parallel, the second device dissipating less power than the first device;

during normal power operation selecting the first device; and

during reduced power operation selecting the second device.

5. The method of claim **4**, wherein the first device and the second device each using a different power supply voltage, the power supply voltage used by the second device being less than the power supply voltage used by the first device.

6. The method of claim **4**, wherein the first device and the second device each operating on a different clock frequency, the clock frequency used by the second device being lower than the clock frequency used by the first device.

7. The method of claim **4**, wherein the first device and the second device each having different functional components, the components in the second device dissipating less power than the components in the first device.

8. The method of claim **4**, wherein the first device and the second device each having a plurality of transistors, the transistors in the second device having a higher threshold voltage than the transistors in the first device.

9. A method for selective allocation of power to elements of a circuit, comprising:

identifying at least one element of the circuit for reduced power dissipation;

selecting the identified at least one element; and

altering at least one input to the selected at least one element, the altered input reducing the power dissipated by the element;

wherein the selecting the at least one element step comprises:

sending a selection signal to a register associated with the identified at least one element; and

holding the selection signal in the register until the register is reset, the selection signal causing the identified at least one element to operate in a reduced power dissipation mode.

10. A method for selective allocation of power to elements of a circuit, comprising:

identifying at least one element of the circuit for reduced power dissipation;

US-PAT-NO: 5781768
DOCUMENT-IDENTIFIER: US 5781768 A

TITLE: Graphics controller utilizing a variable frequency clock

DATE-ISSUED: July 14, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Jones, Jr.; Morris E.	Saratoga	CA	N/A	N/A

US-CL-CURRENT: 713/501

ABSTRACT:

The present invention includes a memory clock system for a graphics controller including a plurality of clock pulse generators, and a clock controller which selects the clock frequency based on the state of the graphics controller functional units.

5 Claims, 4 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

[45] Date of Patent: Jul. 14, 1998

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[75] Inventor: **Morris E. Jones, Jr.** Saratoga, Calif.

[73] Assignee: **Chips and Technologies, Inc.**, San Jose, Calif.

[21] Appl. No.: **625,732**

[22] Filed: **Mar. 29, 1996**

[51] Int. Cl.[6] **G06F 1/06**

[52] U.S. Cl. **395/556**

[58] **Field of Search** 395/556

[56] **References Cited**

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5,586,309	12/1996	Lin	395/556

Primary Examiner—Thomas M. Heckler
Attorney, Agent, or Firm—D'Alessandro & Ritchie

[57] **ABSTRACT**

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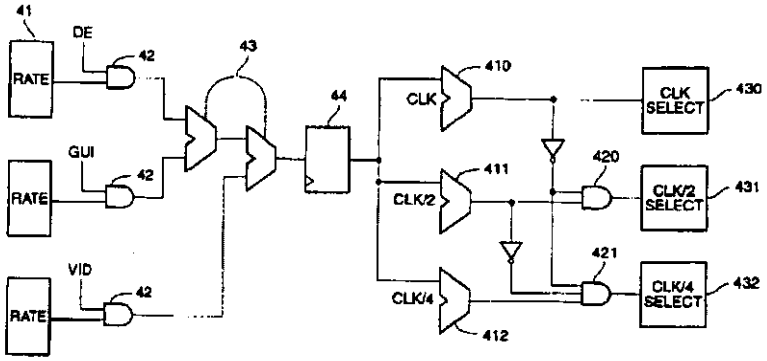
5 Claims, 2 Drawing Sheets



US-PAT-NO: 5996083

DOCUMENT-IDENTIFIER: US 5996083 A

TITLE: Microprocessor having software controllable power consumption

DATE-ISSUED: November 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gupta; Rajiv	Los Altos	CA	N/A	N/A
Raje; Prasad	Fremont	CA	N/A	N/A

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA	N/A	N/A	02

APPL-NO: 08/ 514284

DATE FILED: August 11, 1995

INT-CL: [06] G06F001/00

US-CL-ISSUED: 713/322;713/324

US-CL-CURRENT: 713/322; 713/324

FIELD-OF-SEARCH: 395/750; 395/307 ; 395/310 ; 364/707

REF-CITED:

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL		
4991078	February 1991	Wilhelm et al.	364/200	N/A	N
5142684	August 1992	Perry et al.	395/750	N/A	N/A
5167024	November 1992	Smith et al.	395/375	N/A	N

	U	1	Document ID	Issue Dat	Current	Title
1			US 5881290 A	19990309	717/136	Industrial controller decompiler accommod
2			US 5485623 A	19960116	714/22	Information processor having high speed a
3			US 5692204 A	19971125	713/340	Method and apparatus for computer syste
4			US 5996083 A	19991130	713/322	Microprocessor having software controllab
5			US 5815724 A	19980929	713/322	Method and apparatus for controlling pow

[54] **MICROPROCESSOR HAVING SOFTWARE CONTROLLABLE POWER CONSUMPTION**

[75] Inventors: **Rajiv Gupta**, Los Altos; **Prasad Raje**, Fremont, both of Calif.

[73] Assignee: **Hewlett-Packard Company**, Palo Alto, Calif.

[21] Appl. No.: **08/514,284**

[22] Filed: **Aug. 11, 1995**

[51] **Int. Cl.**[6] **G06F 1/00**

[52] **U.S. Cl.** 713/322; 713/324

[58] **Field of Search** 395/750, 307, 395/310; 364/707

[56] **References Cited**

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5,142,684	8/1992	Perry et al.	395/750
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5,392,437	2/1995	Matter et al.	395/750
5,420,808	5/1995	Alexander et al.	364/707
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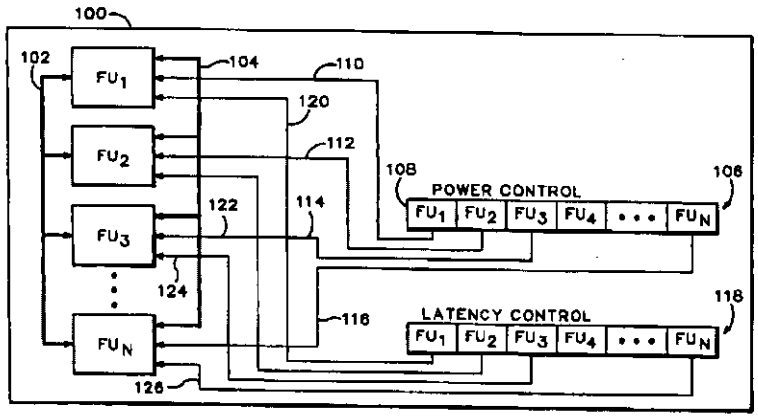
Krick et al., "A 150 MHz 0.6 μm BiCMOS Superscalar Microprocessor," *IEEE Journal of Solid-State Circuits*, vol. 29, No. 12, Dec. 1994, pp. 1455–1458.

Primary Examiner—Ayaz R. Sheikh
Assistant Examiner—Jigar Pancholi

[57] **ABSTRACT**

A microprocessor is provided which includes a power control register for controlling the rate of execution and therefore the power consumption of individual functional units. The power control register includes a plurality of fields corresponding to the functional units for storing values that control the power consumption of each. The power control register fields can be set by software which has the much greater ability to look out into the future to determine whether the functional units will be required. The functional units are responsive to the corresponding power control register field to adjust their rate of execution responsive to the value stored therein. The rate of execution can be controlled in a number of different ways: dividing down the clock; removing power to the functional unit; disabling the sensor and/or buffer driver of one or more of the ports in a multi-ported RAM; removing data from the functional unit; and changing the data bus width responsive to the control register field. The microprocessor also includes a latency control register which assures that the functional unit is operational after the functional unit is placed from a low power state to a more fully operational state by changing the corresponding field in the power control register.

36 Claims, 8 Drawing Sheets



Good Ref

US-PAT-NO: 6219796

DOCUMENT-IDENTIFIER: US 6219796 B1

TITLE: Power reduction for processors by software control of functional units

DATE-ISSUED: April 17, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bartley, David Harold	Dallas	TX	N/A	N/A

US-CL-CURRENT: 713/320; 712/214 ; 713/324

ABSTRACT:

A method of optimizing a computer program for reduced power consumption by a processor (10) having functional units (11d, 11e) that are independently controllable by instructions. The processor's instruction set (FIG. 4) has instructions that may be directed to a particular functional unit (11d, 11e) so as to place that functional unit in a power-down state while not being used during a program segment.

9 Claims, 8 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

	U	1	Document ID	Issue Dat	Current	Title
9			US 5452401 A	19950919	713/322	Selective power-down for high performanc
10			US 5167024 A	19921124	713/322	Power management for a laptop computer
11			US 5825674 A	19981020	713/321	Power control for mobile electronics using
12			US 5719800 A	19980217	713/321	Performance throttling to reduce IC power
13			US 6219796 B	20010417	713/320	Power reduction for processors by softwar

(54) **POWER REDUCTION FOR PROCESSORS BY SOFTWARE CONTROL OF FUNCTIONAL UNITS**

(75) Inventor: **David Harold Bartley**, Dallas, TX (US)

(73) Assignee: **Texas Instruments Incorporated**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/212,190**

(22) Filed: **Dec. 15, 1998**

Related U.S. Application Data

(60) Provisional application No. 60/068,646, filed on Dec. 23, 1997.

(51) **Int. Cl.**[7] **G06F 1/32**

(52) **U.S. Cl.** **713/320**; 713/324; 712/214

(58) **Field of Search** 713/320, 322, 713/324, 323, 300; 709/100, 106; 717/5; 710/1, 100; 708/3, 230; 712/208, 233, 214, 36, 200, 245, 41

(56) **References Cited**

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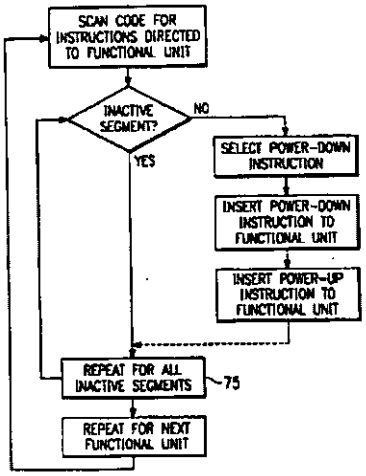
Primary Examiner—Gopal C. Ray

(74) *Attorney, Agent, or Firm*—Robert D. Marshall, Jr.; W. James Brady, III; Frederick J. Telecky, Jr.

(57) **ABSTRACT**

A method of optimizing a computer program for reduced power consumption by a processor (10) having functional units (11d, 11e) that are independently controllable by instructions. The processor's instruction set (FIG. 4) has instructions that may be directed to a particular functional unit (11d, 11e) so as to place that functional unit in a power-down state while not being used during a program segment.

9 Claims, 4 Drawing Sheets



US-PAT-NO: 6256743

DOCUMENT-IDENTIFIER: US 6256743 B1

TITLE: Selective power-down for high performance CPU/system

DATE-ISSUED: July 3, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Chong Ming	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 713/322; 713/310 ; 713/321 ; 713/324

ABSTRACT:

A microelectronic device according to the present invention is made up of two or more functional units, which are all disposed on a single chip, or die. The present invention works on the strategy that all of the functional units on the die are not, and do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device. The present invention on a very rapid basis (typically a half clock cycle), therefore, turns on and off the functional units of the microelectronic device in accordance with the requirements of the program being executed. This power down can be achieved by one of three techniques; turning off clock inputs to the functional units, interrupting the supply of power to the functional units, or deactivating input signals to the functional units. The operation of the present invention results in a very significant reduction in power consumption and corresponding heat dissipation by the microelectronic device as compared to the conventional approach of keeping all functional units operational all of the time.

8 Claims, 9 Drawing figures

Exemplary Claim Number: 1

	U	1	Document ID	Issue Dat	Current	Title
4			US 6282667 B	20010828	713/324	Method and apparatus for selectively pow
5			US 6230279 B	20010508	713/324	System and method for dynamically contr
3			US 5870616 A	19990209	713/324	System and method for reducing power co
7			US 6430693 B	20020806	713/322	Selective power-down for high performanc
2			US 6256743 B	20010703	713/322	Selective power-down for high performanc

(45) Date of Patent: Jul. 3, 2001

(54) **SELECTIVE POWER-DOWN FOR HIGH PERFORMANCE CPU/SYSTEM**

(75) Inventor: **Chong Ming Lin**, Sunnyvale, CA (US)

(73) Assignee: **Seiko Epson Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/069,335**

(22) Filed: **Apr. 29, 1998**

Related U.S. Application Data

(63) Continuation of application No. 08/811,238, filed on Mar. 3, 1997, now Pat. No. 5,787,297, which is a continuation of application No. 08/487,976, filed on Jun. 7, 1995, now Pat. No. 5,655,124, which is a continuation of application No. 07/860,717, filed on Mar. 31, 1992, now Pat. No. 5,452,401.

(51) Int. Cl.[7] **G06F 1/00**

(52) U.S. Cl. **713/322**; 713/310; 713/321; 713/324

(58) Field of Search 713/310, 321, 713/322, 324

(56) **References Cited**

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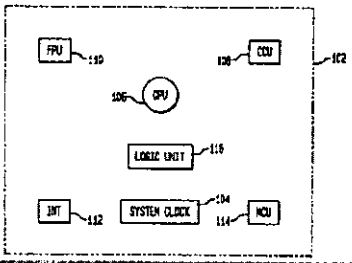
Primary Examiner—Ayaz R. Sheikh
Assistant Examiner—Rupal D. Dharia
(74) *Attorney, Agent, or Firm*—Sterne, Kessler, Goldstein, & Fox, P.L.L.C.

(57) **ABSTRACT**

A microelectronic device according to the present invention is made up of two or more functional units, which are all disposed on a single chip, or die. The present invention works on the strategy that all of the functional units on the die are not, and do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device. The present invention on a very rapid basis (typically a half clock cycle), therefore, turns on and off the functional units of the microelectronic device in accordance with the requirements of the program being executed. This power down can be achieved by one of three techniques; turning off clock inputs to the functional units, interrupting the supply of power to the functional units, or deactivating input signals to the functional units. The operation of the present invention results in a very significant reduction in power consumption and corresponding heat dissipation by the microelectronic device as compared to the conventional approach of keeping all functional units operational all of the time.

8 Claims, 6 Drawing Sheets



US-PAT-NO: 5677849

DOCUMENT-IDENTIFIER: US 5677849 A

TITLE: Selective low power clocking apparatus and method

DATE-ISSUED: October 14, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Smith; Stephen Arthur	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 713/300; 713/321 ; 713/322 ; 713/324

ABSTRACT:

A selective low power clocking apparatus and method is used to reduce power consumption by an electronic system or integrated circuit that is coupled to an external system via a system bus which is configured to selectively transmit or receive signals from the electronic system or integrated circuit. The electronic system or integrated circuit includes a plurality of sub-circuits or functional blocks. Each sub-circuit or functional block is configured to operate under control of a clock signal and further includes an apparatus for holding or rejecting the clock signal. Once each sub-circuit within the electronic system or integrated circuit rejects the clock signal, the clock signal to that sub-circuit is disabled. The arbiter circuit continuously monitors the system bus. Upon detecting that the external system needs to transmit or receive signals from the electronic system or integrated circuit, the arbiter re-enables the clock signal to the sub-circuits which are required for the transmission or reception.

28 Claims, 2 Drawing figures

Exemplary Claim Number: 1

	U	1	Document ID	Issue Dat	Current	Title
21	☐	☐	US 6357011 B	20020312	713/300	Bus-powered computer peripheral with su
22	☐	☐	US 6345362 B	20020205	713/300	Managing Vt for reduced power using a st
23	☐	☐	US 6081901 A	20000627	713/300	System and method for dynamically contr
24	☐	☐	US 5805907 A	19980908	713/300	System and method for reducing power co
25	☐	☐	US 5677849 A	19971014	713/300	Selective low power clocking apparatus ar

[45] Date of Patent: Oct. 14, 1997

[54] **SELECTIVE LOW POWER CLOCKING APPARATUS AND METHOD**

[75] Inventor: Stephen Arthur Smith, Palo Alto, Calif.

[73] Assignee: Cirrus Logic, Inc., Fremont, Calif.

[21] Appl. No.: 581,480

[22] Filed: Dec. 28, 1995

Related U.S. Application Data

[63] Continuation of Ser. No. 148,378, Nov. 8, 1993, abandoned.

[51] Int. Cl.[6] G06F 1/32

[52] U.S. Cl. 364/492; 364/707; 395/750

[58] Field of Search 364/141, 492, 364/493, 707, 569; 395/550, 750; 377/81

[56] **References Cited**

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4,615,005	9/1986	Maejima et al.	364/707 X
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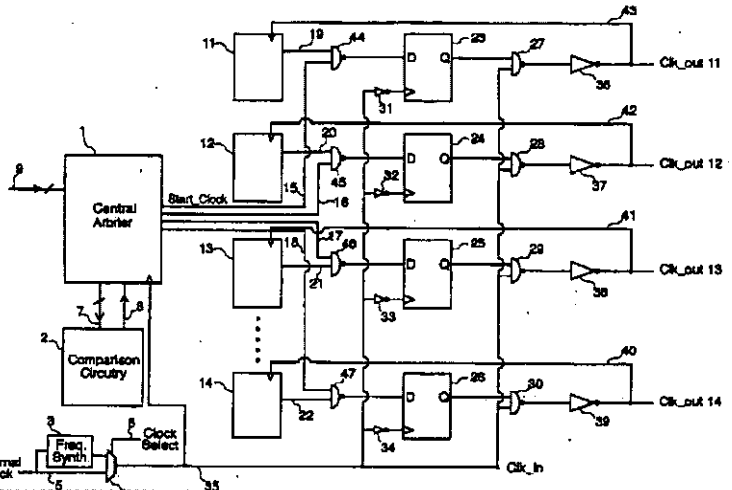
5,162,667	11/1992	Yasui et al.	307/272.2
5,276,889	1/1994	Shiraishi et al.	395/750
5,452,401	9/1995	Lin	395/750

Primary Examiner—Emanuel T. Voeltz
Assistant Examiner—M. Kemper
Attorney, Agent, or Firm—Thomas B. Haverstock; Robert P. Bell; J. P. Violette

[57] **ABSTRACT**

A selective low power clocking apparatus and method is used to reduce power consumption by an electronic system or integrated circuit that is coupled to an external system via a system bus which is configured to selectively transmit or receive signals from the electronic system or integrated circuit. The electronic system or integrated circuit includes a plurality of sub-circuits or functional blocks. Each sub-circuit or functional block is configured to operate under control of a clock signal and further includes an apparatus for holding or rejecting the clock signal. Once each sub-circuit within the electronic system or integrated circuit rejects the clock signal, the clock signal to that sub-circuit is disabled. The arbiter circuit continuously monitors the system bus. Upon detecting that the external system needs to transmit or receive signals from the electronic system or integrated circuit, the arbiter re-enables the clock signal to the sub-circuits which are required for the transmission or reception.

28 Claims, 2 Drawing Sheets



DOCUMENT-IDENTIFIER: US 5423047 A
TITLE: Methods and apparatus for using address transition detection to reduce power consumption

------ KWIC ------

DEPR:
FIG. 4 illustrates the timing for power reduction of circuit elements of the device 12. The ATD & POWER 24 detects address transitions over the address portion 16 of the bus 14, and generates signals to selectively enable and disable circuit elements and latch data from the memory array 20. The timing of address signals received (ADDR) and the data transmitted (DATA) is shown, along with the ATD.sub.-- MP signal 61, the SALEN signal 35, the ATD.sub.-- PWR signal 60, the DBEN signal 31, and the SAEN signal 34.

read Latch circuit

US-PAT-NO: 6343043
DOCUMENT-IDENTIFIER: US 6343043 B1

TITLE: Dynamic random access memory

DATE-ISSUED: January 29, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kai; Yasukazu	Miyazaki	N/A	N/A	JPX
Gotoh; Takeshi	Tokyo	N/A	N/A	JPX

US-CL-CURRENT: 365/222,365/196

ABSTRACT:

In order to reduce power consumption in a dynamic random access memory (DRAM), block selection information RBDATA indicating whether or not individual blocks in a memory cell array require a refresh is stored at means for latching 20-1 and 20-2. A circuit for operation prohibition 30 compares a portion RA8 of a refresh address output by a refresh counter 6 with refresh block specification signals RB (0) and RB (1) output by the circuit for latching 20-1 and 20-2, makes a decision as to whether or not the block indicated by the refresh address needs to be refreshed and prohibits an operation of an RAS system circuit 11 if it is decided that the block does not need to be refreshed. Thus, a self refresh is not performed for a block that does not need to be refreshed to achieve a reduction in power consumption.

20 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 20

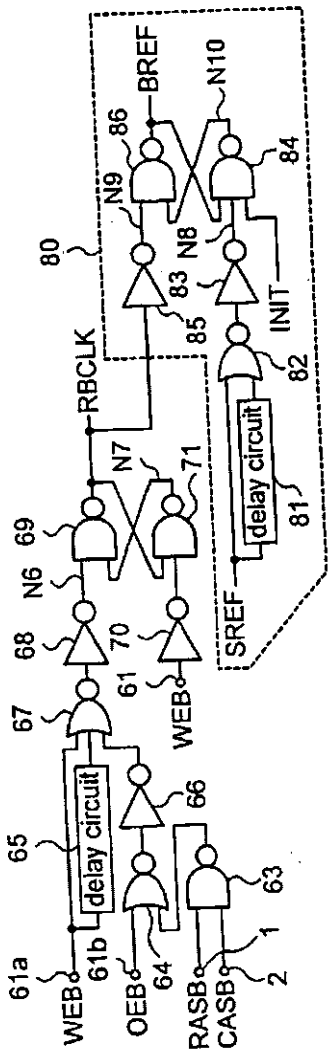


FIG.15

DOCUMENT-IDENTIFIER: US 5544101 A
TITLE: Memory device having a latching multiplexer and a multiplexer block therefor

------ KWIC ------

DEPR:
The present invention teaches a memory device architecture having latches at the multiplexer block 14 reducing power consumption. Power consumption is reduced whether or not differential signals are implemented although the power savings is greater when differential signals are used in the multiplexer block 14. The memory device architecture of the present invention is beneficial for all memories, but is especially beneficial for memories implemented using large cell arrays.

[54] **MEMORY DEVICE HAVING A LATCHING MULTIPLEXER AND A MULTIPLEXER BLOCK THEREFOR**

[75] Inventor: **Theodore W. Houston**, Richardson, Tex.

[73] Assignee: **Texas Instruments Inc.**, Dallas, Tex.

[21] Appl. No.: **219,609**

[22] Filed: **Mar. 28, 1994**

[51] Int. Cl.[6] G11C 7/00; H03J 3/04

[52] U.S. Cl. 365/189.02; 365/189.05; 365/230.02; 365/230.08; 327/407

[58] Field of Search 365/189.02, 189.05, 365/230.02, 230.08; 327/407, 408

[56] **References Cited**

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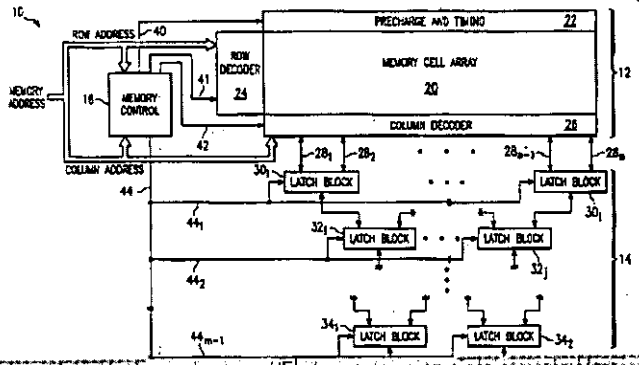
IEEE Journal of Solid-State Circuits, Bernard K. Gunther, "An Integrated Pre-Access Architecture for CMOS SRAM", vol. 27, No. 6, pp. 901-907, Jun. 1992.

Primary Examiner—David C. Nelms
Assistant Examiner—Son Dinh
Attorney, Agent, or Firm—William B. Kempler; Richard L. Donaldson

[57] **ABSTRACT**

A memory device (10) is provided which includes a memory array (12), a multiplexer block (14) and a control block (16). The memory array (12) is operable to provide a plurality of memory array outputs ($28_1 \ldots 28_n$) responsive to a memory address (MEMORY ADDRESS). Each memory array output ($28_1 \ldots 28_n$) represents a data state of a memory cell. The multiplexer block (14) comprises at least one latch block ($30_1 \ldots 30_n$, $32_1 \ldots 32_j$, 34_1, 34_2, and 36) arranged in at least one stage. The multiplexer block is coupled to the plurality of memory array outputs ($28_1 \ldots 28_n$). The multiplexer block (14) is operable to provide a multiplexer block output (38) representing a data state of a desired memory cell corresponding to the memory address (MEMORY ADDRESS) responsive to a plurality of multiplexer control signals ($44_1 \ldots 44_m$). Each latch block is operable to receive a plurality of input signals, operable to retain a plurality of data states and operable to provide an output signal. A control block (16) is coupled to the memory array (12) and to the multiplexer block (14). The control block (16) is operable to determine from the memory address (MEMORY ADDRESS) whether the data state of the desired memory cell is retained by a latch block in the multiplexer block (14) and operable to generate the plurality of multiplexer control signals ($44_1 \ldots 44_m$).

28 Claims, 3 Drawing Sheets



US-PAT-NO: 6173408

DOCUMENT-IDENTIFIER: US 6173408 B1

TITLE: Processor

------ KWIC ------

US Reference Patent Number - URPN (4):

5787297

	U	1	Document ID	Issue Dat	Current	Title
1			US 6430693 B	20020806	713/322	Selective power-down for high performanc
2			US 6173408 B	20010109	713/322	Processor
3			US 6282663 B	20010828	713/320	Method and apparatus for performing pow
4			US 6085325 A	20000704	713/300	Method and apparatus for supporting pow
5			US 6496925 B	20021217	712/244	Method and apparatus for processing an e

(54) **PROCESSOR**

(75) Inventors: **Takuya Jimbo; Akihiko Ohtani, Toshiyuki Araki,** all of Osaka (JP)

(73) Assignee: **Matsushita Electric Industrial Co., Ltd.,** Osaka (JP)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/145,646**

(22) Filed: **Sep. 2, 1998**

(30) **Foreign Application Priority Data**

Sep. 3, 1997 (JP) 9-238014

(51) **Int. Cl.**[7] **C06F 1/32**

(52) **U.S. Cl.** **713/322**; 712/32; 713/600

(58) **Field of Search** 713/322, 601, 713/300, 320, 324, 323, 321, 500, 600; 712/23, 36, 32; 710/100

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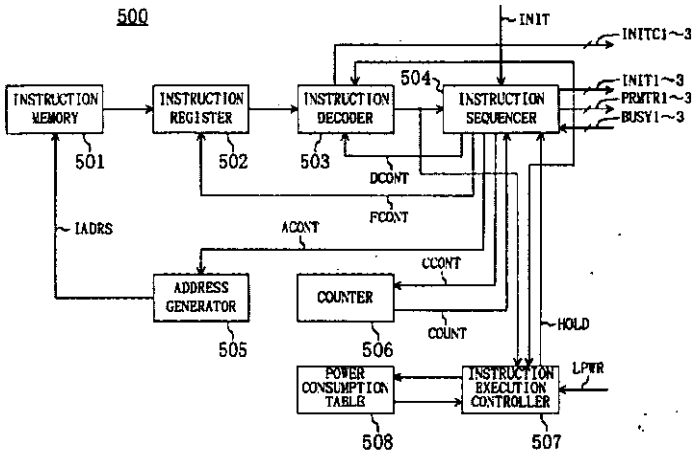
Primary Examiner—John A. Follansbee
Assistant Examiner—Walter Benson
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

An operation controller, an operation unit and a memory are provided. The operation controller always receives a non-gated clock signal from a clock controller. When an operation initiating signal and a parameter signal indicating resources to be used in the operation unit are generated by a microcontroller, the operation controller asserts a request signal. In response to the request signal, respective gated clock signals are supplied from the clock controller to the operation unit and to the memory. The operation controller determines whether or not a status signal supplied from the operation unit satisfies a predetermined end condition. If the signal satisfies the end condition, the operation controller negates the request signal. As a result, the supply of the clock signals to the operation unit and to the memory is stopped.

12 Claims, 20 Drawing Sheets



US-PAT-NO: 6097378

DOCUMENT-IDENTIFIER: US 6097378 A

TITLE: Video display apparatus with audio circuitry and a method for controlling power therein

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US Reference Patent Number - URPN (9):

5787297

	U	1	Document ID	Issue Dat	Current	Title
3			US 6282663 B	20010828	713/320	Method and apparatus for performing pow
4			US 6085325 A	20000704	713/300	Method and apparatus for supporting pow
5			US 6496925 B	20021217	712/244	Method and apparatus for processing an e
6			US 6535905 B	20030318	709/108	Method and apparatus for thread switchin
1			US 6097378 A	20000801	345/211	Video display apparatus with audio circuitr

[45] Date of Patent: Aug. 1, 2000

[54] **VIDEO DISPLAY APPARATUS WITH AUDIO CIRCUITRY AND A METHOD FOR CONTROLLING POWER THEREIN**

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[21] Appl. No.: **08/899,385**

[22] Filed: **Jul. 23, 1997**

[30] **Foreign Application Priority Data**

Jul. 23, 1996 [KR] Rep. of Korea 96-29792

[51] Int. Cl.[7] G09G 5/00

[52] U.S. Cl. 345/211; 345/210; 345/212; 345/213

[58] Field of Search 345/204, 210, 345/211, 212, 213, 214; 381/110, 120, 123; 348/632, 633, 729, 730; 358/189, 190; 713/320, 323, 324

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Attorney, Agent, or Firm—Robert E. Bushnell, Esq.

[57] **ABSTRACT**

In one arrangement of a video display apparatus according to the present invention, an audio power supply, which separated from a constant voltage generator, is directly connected to a main power supply and supplies power to an audio circuit. A microcontroller generates an audio power control signal in response to key input data entered from a key input unit. An audio power controller is provided to shut off the audio power supplied to the audio circuit in response to the audio power control signal from the microcontroller. In another arrangement, the audio power supply is connected to an auxiliary power supply for supplying power to the microcontroller. Thus, the supplying of the audio power to the audio circuit can be controlled independent of the video circuitry and in accordance with user's need.

9 Claims, 8 Drawing Sheets